What is Claimed is:

[c1] A method of forming a plurality of conductive structures on a substrate comprising the steps of:

forming a first semiconductor structure of a first conductivity type, a second semiconductor structure of a second conductivity type, and a third semiconductor structure on a substrate, said third semiconductor structure being disposed between said first and second semiconductor structures and being separated therefrom by an insulator structure;

depositing an interconnect layer over at least said first, second and third semiconductor structures;

forming a planarizing conductor on said interconnect layer, said planarizing conductor having etch characteristics similar to those of said interconnect layer and said first and second semiconductor structures, but different from those of said insulator structure; and

patterning and etching said planarizing conductor, said interconnect layer, and said first and second semiconductor structures so that each has at least one lateral dimension that is substantially the same.

[c2] The method of Claim 1 wherein said first and second semiconductor structures are formed utilizing a double angled implant such that vertical surfaces of a polysilicon-containing or semiconducting layer formed abutting said insulator structure are oppositely doped, while horizontal surfaces of said polysilicon-containing or semiconducting layer are doubly doped.

[c3] The method of Claim 2 wherein said polysilicon-containing layer is comprised of poly-crystalline silicon.

[c4] The method of Claim 2 wherein said polysilicon-containing layer is comprised of a poly-crystalline silicon-germanium alloy.

[c5] The method of Claim 2 wherein said double angled implant is performed so as to provide implant regions whose final dopant concentration is on the order of from about $1x10^{19}$ to about $1x10^{21}$ atoms/cm^3.

[c6] The method of Claim 1 wherein said insulator structure includes a gate dielectric and a hard mask.

[c7] The method of Claim 1 wherein said interconnect layer is a metallic layer which is capable

of preventing dopant diffusion into said first and second semiconductor structures.

[c8] The method of Claim 1 wherein said planarizing conductor is comprised of a polysilicon-containing material, a conductive metal, a conductive metal alloy or a semiconducting material.

[c9] The method of Claim 8 wherein said planarizing conductor is comprised of poly-crystalline silicon or a poly-crystalline silicon-germanium alloy.

[c10] The method of Claim 1 further comprising annealing said interconnect layer so as to convert said layer into a metal silicide or metal nitride.

[c11] The method of Claim 10 wherein said annealing is carried out at a temperature of about 700Â°C or higher and in the presence of inert gas atmosphere.

[c12] An asymmetric field effect transistor (FET) comprising:
a p-type gate portion and an n-type gate portion on a vertical semiconductor body;
an interconnect between said p-type gate portion and said n-type gate portion; and
a planarizing structure above said interconnect.

[c13] The asymmetric FET of Claim 12 wherein said p-type gate portion, said n-type gate portion, said interconnect, and said planarizing structure have a lateral dimension that is substantially the same.

[c14] The asymmetric FET of Claim 12 wherein said p-type gate portion, said n-type gate portion and said planarizing structure are composed of a polysilicon-containing material or a semiconducting material.

[c15] The asymmetric FET structure of Claim 14 wherein said polysilicon-containing material comprises polySi or polySiGe.

[c16] The asymmetric FET of Claim 12 wherein said interconnect is highly resistant to dopant diffusion.

[c17] The asymmetric FET of Claim 12 wherein said interconnect is a conductive metal, metal silicide or metal nitride, or a semi-metal.

[c18] The asymmetric FET of Claim 12 wherein said planarizing structure is doped polysilicon.

[c19] The asymmetric FET of Claim 12 wherein said vertical semiconductor body has a gate dielectric present on vertical sidewalls of said body.

[c20] The asymmetric FET of Claim 12 wherein said vertical semiconductor body has a hard mask present on an upper surface.

[c21] The asymmetric FET of Claim 20 wherein said hard mask is comprised of an oxide, nitride, oynitride or multilayers thereof.

[c22] The asymmetric FET of Claim 12 wherein said n-type gate portion is comprised of N-doped polysilicon and said p-type gate portion is comprised of P-type polysilicon.

[c23] The asymmetric FET of Claim 12 wherein said vertical semiconductor body is formed atop a substrate, said substrate comprises an upper insulating portion and a lower semiconducting portion.

[c24] The asymmetric FET of Claim 23 wherein said vertical semiconductor body and said substrate are components of a silicon-on-insulator material.

[c25] The asymmetric FET of Claim 12 wherein said planarizing material is a metal or metal alloy.

[c26] The asymmetric FET of Claim 12 further comprising source/drain regions in areas adjacent to the vertical semiconductor body.

[c27] The asymmetric FET of Claim 26 wherein said source/drain regions are doped so as to have either donor or acceptor impurities.

[c28] An asymmetric field effect transistor (FET) comprising:
a p-type gate portion and an n-type gate portion on a vertical single crystal Si semiconductor body, said p-type and n-type gate portions are composed of polysilicon;
a metal silicide interconnect between said p-type gate portion and said n-type gate portion; and
a planarizing doped polysilicon layer above said interconnect.